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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,177	06/30/2003	Anthony R Bonaccio	BUR920020059US1	1176

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EXAMINER
KIM, KEVIN

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,177	BONACCIO ET AL.	
	Examiner	Art Unit	
	Kevin Y. Kim	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 19-30* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-17,19-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Janesch et al (US 6,097,768).

Claim 1.

Janesch et al discloses a phase adjustable clock circuit comprising:

means (220) for generating a first and a second clock signal (I and Q); and

means (164) for adjusting the phase of said first and second clock signals.

Claim 2.

The unadjusted phases of said first and second clock signals are 90 degrees apart as they are in quadrature relation.

Claims 3.

Depending on the phase error between the received signal and each of the I and Q clock signals, the phase of said first clock signal is adjusted in a phase range of +/- 90 degrees and the phase of the second clock signal is not adjusted.

Claims 4.

The center of the phase range of said adjusted first clock signal is offset +/-90 degrees from the phase of said second clock signal as they are in quadrature relation.

Claims 5.

The amount of phase adjustment of said first clock signal is a function of magnitude of a control voltage (VCO) applied to said phase adjustment circuit.

Claim 6.

The phase of said first clock signal is adjusted in a phase range of +/- 90 degrees and the phase of the second clock signal is adjusted in a phase range of +/- 90 degrees.

Claim 7.

The center of the phase range of said adjusted first clock signal is offset +/-90 degrees from the center of the phase range of said adjusted second clock signal as they are in quadrature relation.

Claim 8.

Depending on the phase error between the received signal and each of the I and Q clock signals, the amounts of phase adjustment of said first and second clock signals are the same and are a function of the magnitude and polarity of a control voltage applied to said phase adjustment circuit.

Claim 9.

Janesch et al discloses a phase adjustable clock circuit comprising:

means (220) for generating a first clock signal (I before adjustment) and a second clock signal (Q before adjustment); and

means (164) for receiving said first clock signal and for generating a third clock signal (I after adjustment) from said first clock signal and means (164) for receiving said second clock signal and for generating a fourth clock signal (Q after adjustment), wherein at least one of said third and said fourth clock signals differ in phase from said first and said second clock signal respectively.

Claim 10.

The phases of said first and second clock signals are 90 degrees apart as they are in quadrature relation.

Claim 11.

Depending on the phase error between the received signal and each of the I and Q clock signals, the phase of said third clock signal differs in a phase range of +/- 90 degrees from the phase of said first clock signal and the phases of the second clock signal and fourth clock signals are the same.

Claim 12.

The center of the phase range of said third clock signal is offset +/-90 degrees from the phase of said fourth clock signal as they are in quadrature relation.

Claim 13.

The phase difference between said first clock signal and said third clock signal is a function of magnitude of a control voltage (VCO) applied to said phase adjustment circuit.

Claim 14.

Depending on the phase error between the received signal and each of the I and Q clock signals, the phase of said third clock signal differs in a phase range of +/- 90 degrees from the phase of said first clock signal and the phase of said fourth clock signal differs in a phase range of +/- 90 degrees from the phase of said second clock signal.

Claim 15.

The center of the phase range of said third clock signal is offset +/-90 degrees from the center of the phase range of said fourth clock signal as they are in quadrature relation.

Claim 16.

An amount of phase difference between said first and third clock signals is the same as an amount of phase difference between said second and fourth clock signals and is a function of the magnitude and polarity of a control voltage (VCO) applied to said phase adjustment circuit.

Claim 17.

Janesch et al discloses a clock and data recovery circuit comprising:

means (220) for generating a first and a second clock signal;

means (164) for receiving said first clock signal and for generating a third clock signal from said first clock signal and means (164) for receiving said second clock signal and for generating a fourth clock signal, wherein at least one of said third and said fourth clock signals differ in phase from said first and said second clock signal respectively;

means (164) for receiving said third and fourth clock signals and a serial data

stream (Received signal) and for generating a reconstructed serial data stream and a phase error signal;

means (166) for receiving said phase error signal and for generating a phase adjustment signal (167) and means (210) for receiving said phase adjustment signal by said clock generation circuit in a feedback loop to adjust the phases of said first and second clock signals.

Claim 19.

Since the phases of the received data and I clock signal are compared, the phase of said third clock signal (i.e., I clock signal) is adjustable in a phase range centered on the high/low transition of said serial data stream.

Claim 20.

The amount of phase adjustment of said third clock signal is a function of the magnitude and polarity of a control voltage (VCO) applied to said phase adjustment circuit.

Claim 21.

When the received signal is in lock with the third clock signal, the phase of said third clock signal is aligned to the zero transition of said serial data stream.

Claim 22.

In order to lock the fourth clock signal with the received signal, the phase of said fourth clock signal is adjusted in a phase range centered on the zero transition of said serial data stream.

Claim 23.

The amount of phase adjustment of said fourth clock signal is a function of the magnitude and polarity of a control voltage (VCO) applied to said phase adjustment circuit.

Claim 24.

The phases of said first and second clock signals are 90 degrees apart as they are in a quadrature relation.

Claim 25.

Depending on the phase error between the received signal and each of the I and Q clock signals, the phase of said third clock signal differs in a phase range of +/- 90 degrees from the phase of said first clock signal and the phases of the second clock signal and fourth clock signals are the same.

Claim 26.

The center of the phase range of said third clock signal is offset +/-90 degrees from the phase of said fourth clock signal as they are in a quadrature relation.

Claim 27.

The phase difference between said first clock signal and said third clock signal is a function of the magnitude and polarity of a control voltage (VCO) applied to said phase adjustment circuit.

Claim 28.

Depending on the phase error between the received signal and each of the I and Q clock signals, the phase of said third clock signal differs in a phase range of +/- 90 degrees

from the phase of said first clock signal and the phase of said fourth clock signal differs in a phase range of +/- 90 degrees from the phase of said second clock signal.

Claim 29.

The center of the phase range of said third clock signal is offset +/-90 degrees from the center of the phase range of said fourth clock signal as they are in a quadrature relation.

Claim 30.

Depending on the phase error between the received signal and each of the I and Q clock signals, an amount of phase difference between said first and third clock signals is the same as an amount of phase difference between said second and fourth clock signals and is a function of the magnitude and polarity of a control voltage applied to said phase adjustment circuit.

Allowable Subject Matter

3. Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dalmia (US 6,211,741) and Boerstler (US 6,480,049) teaches a multiphase clock generator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Y. Kim whose telephone number is 571-272-3039. The examiner can normally be reached on 8AM --5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

October 13, 2006

AU 2611

Kevin Kim

KEVIN KIM
PRIMARY PATENT EXAMINER